HEWLETT hp PACKARD

BENCH BRIEFS

SERVICE INFORMATION FROM HEWLETT-PACKARD

JANUARY-FEBRUARY 1977

LOGIC SYMBOLS SUMMARY

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Since the articles on Logic Symbols were spread over almost 9 months, and many new subscribers did not receive all the pertinent issues, I felt it would be appropriate to highlight some of the material from the series and expand on other items that had been originally edited out. Also, if you want to obtain a copy of the IEEE 91-1973 Standard, write to:

American National
Standards Institute
1430 Broadway
New York, N.Y. 10018

QUALIFIERS

Qualifiers are that portion of the symbol (either rectangular or distinctive shaped) that denotes the logic function.

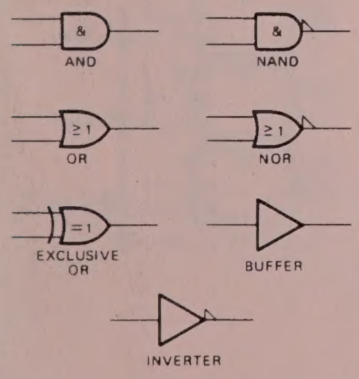
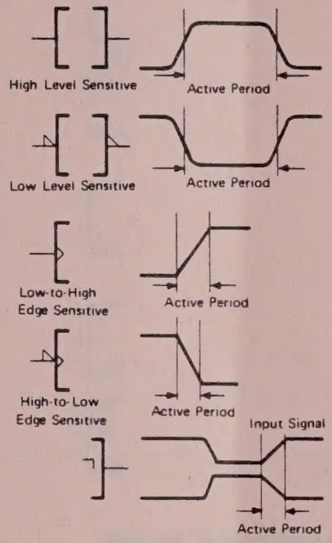


Figure 1. Qualifiers

INDICATOR SYMBOLS

Indicator symbols identify the active state or level of a symbol's input or output with respect to its definition. For our purposes, we will assume positive logic (i.e., the more positive voltage level (H) is a logic 1).



ACTIVE HIGH inputs and outputs are indicated by the absence of the polarity indicator (◺) or negation symbol (o).

ACTIVE LOW inputs and outputs are indicated by the presence of the polarity indicator (◺) or negation symbol (o).

EDGE SENSITIVE (Dynamic) inputs are indicated by the presence of the dynamic indicator symbol (▷).

OUTPUT DELAY indicator symbol (┐) shows that an output becomes effective when the signal that initiated that change returns to its opposite state.

Figure 2. Indicator Symbols

CONTIGUOUS BLOCKS

Two symbols may share a common boundary parallel or perpendicular to the direction of signal flow. Note that in the examples shown in Figure 3, there is generally no logic connection across a horizontal line; however, there is always a logic connection across a vertical line. An exception to this is the Common Control Block (Figure 4) where there is a logic connection across a horizontal line.

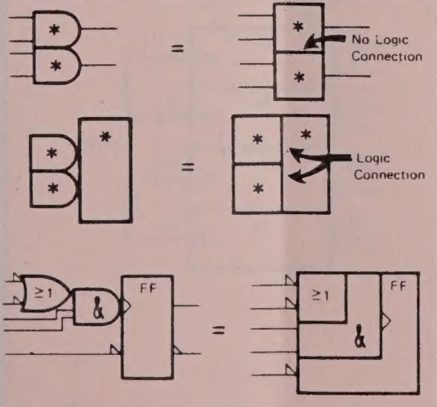


Figure 3. Contiguous Blocks

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COMMON CONTROL BLOCK

The Control Block is used in conjuction with an array of related symbols in order to group common logic lines. Figure 4 shows how the Control Block is usually represented.

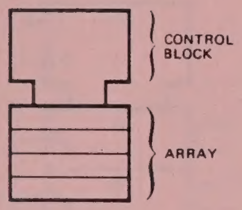


Figure 4. Common Control Block

Figure 5 shows a quad D-Type flip-flop with reset. This can be redrawn by combining what has been shown previously in Figures 3 and 4 about Contiguous Blocks and Common Control Blocks. The result is shown in Figure 6.

Note that the more complex representation shown in Figure 5 might be used when the flip-flops are functionally scattered around the schematic (not used as a quad unit).

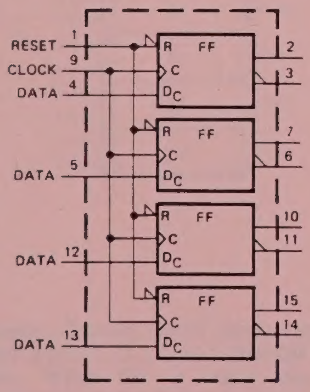
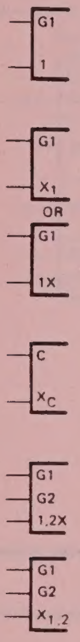


Figure 5. Quad D-Type Flip-Flop

DEPENDENCY NOTATION

Dependency Notation is a way to simplify symbols for complex IC elements by defining the existence of an AND relationship between inputs, or by the AND conditioning of an output by an input without actually showing all the elements and interconnections involved. The following examples use the letter "C" for control and "G" for gate. The dependent input is labeled with a number that is either prefixed (e.g. 1X) or subscripted (e.g.X_1). They both mean the same thing.



The input that controls or gates other inputs is labeled with a "C" or a "G", followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, "1" is controlled by "G1".

When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.

If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.

If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example "X" is controlled by "G1" and "G2".

Figure 7. Dependency Notation, General Form Using Numbers

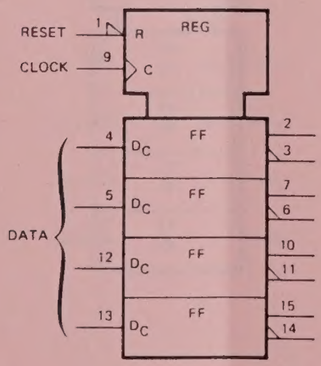


Figure 6. Quad D-Type Latch (Combined)

Note that many times a controlled line may already be labeled with a number; as for example, a coder. In this case, the controlling or gating input will be labeled with a letter. See Figure 8.

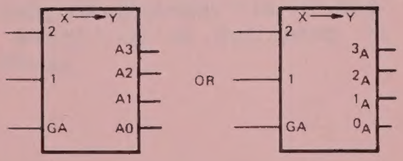
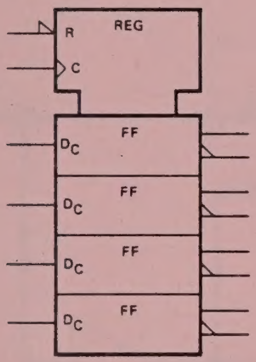


Figure 8. Dependency Notation, Coder Example Using Letters

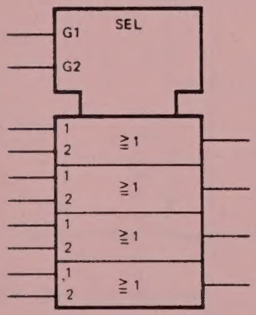
COMPLEX DEVICES

Figures 9 through 12 show how the basic symbols we've looked at can be combined in various ways to illustrate the behavior of fairly complex devices.



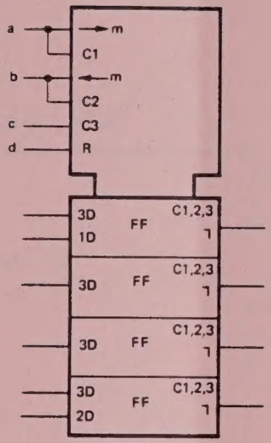
Register control block used to illustrate a quad D-type latch. There is a common active-low reset (R), and a common edge-triggered control input (C). Since there is only one dependency relationship, the controlling input is not numbered and the controlled functions (D) are subscripted with a C.

Figure 9. Quad D-Type Latch Example



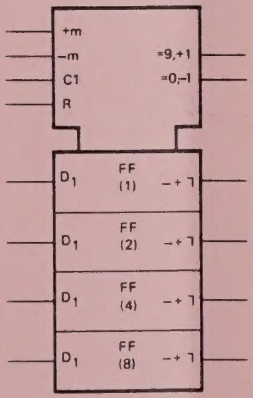
Selector Control Block used to simplify AND portion of a quad AND-OR select gate. When G1 is high, the data presented at the "1" inputs will be gated through. When G2 is high, the data presented at the "2" inputs will be gated through.

Figure 10. And-Or Selector Example



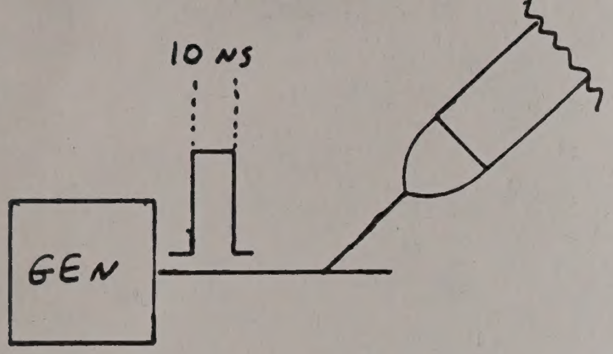
Shift Register Control Block used to show common inputs to a bidirectional shift register. Notice that "→m" means shift the contents to the right or down by "m" units. And "←m" means shift the contents to the left or up by "m" units. Note: If m = 1, it may be omitted. Inputs "a" and "b" are each single IC pins that have two functions. Input "a" enables one of the inputs to the top D-type flip-flop (1D), and also shifts the register contents down one unit. Input "b" enables one of the inputs to the bottom flip-flop (2D), and also shifts the register contents up one unit. Input "c" loads all four flip-flops in parallel (3D). Input "d" is a common reset. The output delay indicator is used because these are master-slave flip-flops.

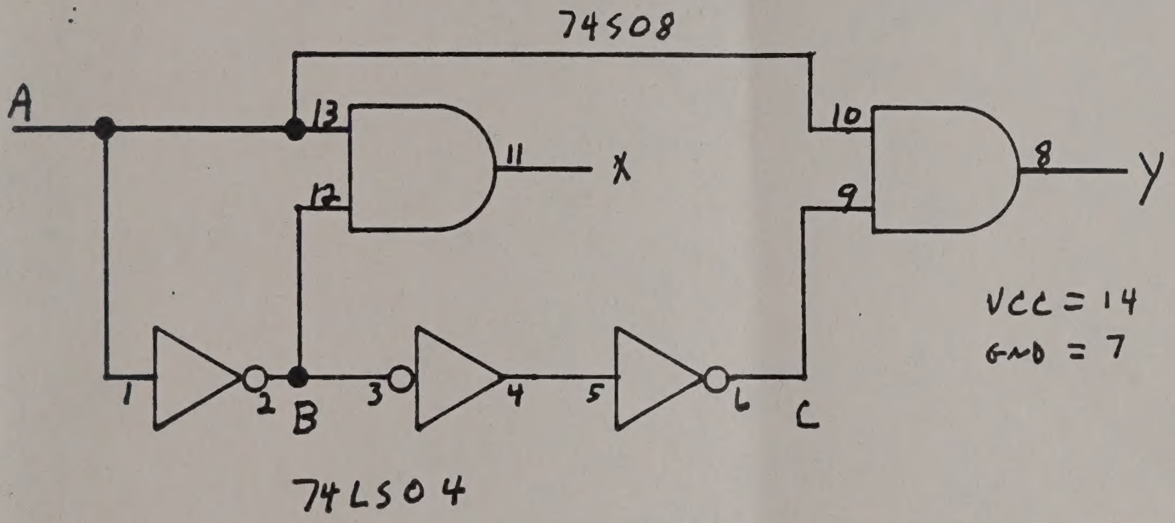
Figure 11. Shift Register Example



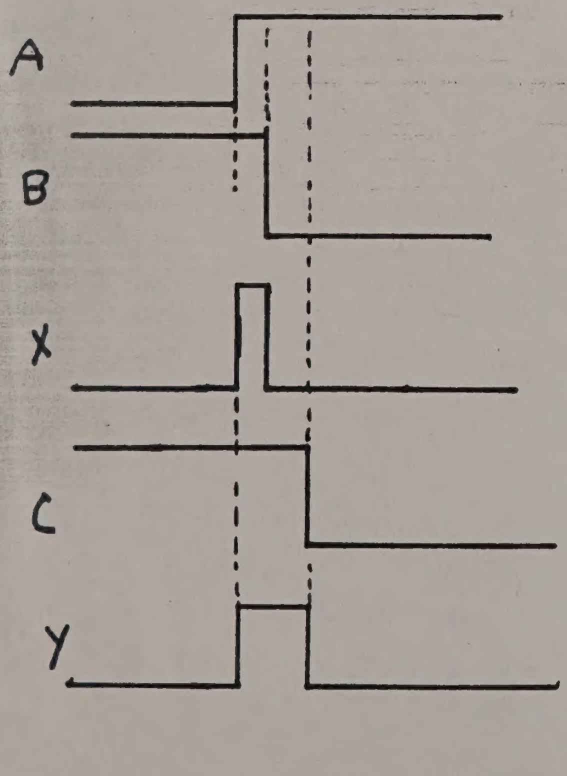
Counter Control Block used to show common inputs to a Presettable Decade Up/Down Counter. Notice that "+m" means count up (increment the count) by "m"; "-m" means count down by "m". Note: if m = 1, it may be omitted. Since the D-type flip-flops are master-slave, the output delay indicator is used. The "=9, + 1" and "=0, -1" notation defines when the carry and borrow outputs are generated. They also define it as a decade counter; a binary counter would have carry indicated with "=15, +1". Flip-flop weighting is indicated in parenthesis.

Figure 12. Up/Down Counter Example





VCC = 14
GND = 7



CONSTRUCT CIRCUIT ON
A PIECE OF PERF-BOARD, 8 X 11 HOLES
USE SOCKETS FOR IC's.